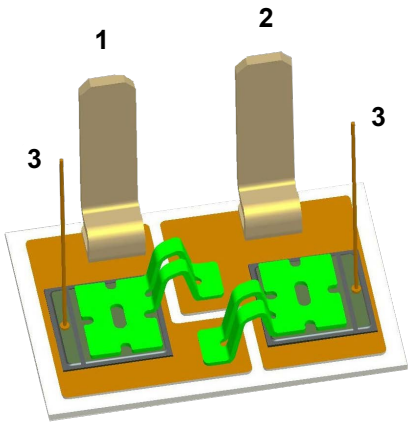
Antiparallel Thyristor Module, 100A
(DBC Module, open-frame type)
Snubberless

FEATURES

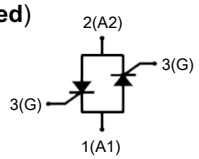
- Glass passived thyristor chips
- Low thermal resistance with clip bonding
- Low thermal resistance for DBC package
- High commutation capability
- Packages are RoHS compliant

APPLICATIONS

- DC motor control
- Temperature control
- Lighting control
- Soft starters



100KQxxK (Insulated)



MAIN FEATURES		
SYMBOL	VALUE	UNIT
$I_{T(RMS)}$	100	A
V_{DRM}/V_{RRM}	1200 to 1600	V
V_{RSM}	1300 to 1700	V
$I_{GT(Q1)}$	max.80	mA

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	TEST CONDITIONS		VALUE	UNIT
RMS on-state current (full sine wave)	$I_{T(RMS)}$	W1C Sin.180°	T_c=80ºC	100	A
			T_c=100ºC	70	
Non repetitive surge peak on-state current (full cycle)	I_{TSM}	F = 50 Hz, V_R = 0.6 V_{RRM},T_j = 25°C	t=10 ms	1200	A
		F = 50 Hz, V_R = 0.6 V_{RRM},T_j = 125°C	t=10 ms	840	
I^2t Value for fusing	I^2t	T_j = 25ºC	t=10 ms	1000	A^2s
		T_j = 125ºC	t=10 ms	720	
Critical rate of rise of on-state current I_G = 2xI_{GT}, t_r≤100ns	dI/dt	V_D = 66.7% V_{DRM}, t_p = 200µs, I_G = 0.3A, dI_G/dt = 0.3A/µs	T_j=125ºC	100	A/µs
Turn-Off Time	tq		T_j=125ºC	8	A
Gate-controlled delay time	t_{gd}	I_G = 1A ; di_G/dt = 1A/µs	T_j=25ºC	1	µs
Gate-controlled rise time	t_{gr}	V_D = 0.67*V_{DRM}		2	
Storage temperature range	T_{stg}			- 40 to + 150	ºC
Operating junction temperature range	T_j			- 40 to + 125	

◎ ELECTRICAL CHARACTERISTICS (T_J= 25 ºC unless otherwise specified)

SNUBBERLESS and Logic level (3 quadrants)					
SYMBOL	TEST CONDITIONS	QUADRANT		VALUE	Unit
I_{GT}(1)	V_D = 12 V, R_L = 30Ω	I - II - III	MAX.	80	mA
V_{GT}		I - II - III		2	V
V_{GD}	V_D = V_{DRM}, R_L = 3.3KΩ T_j = 125°C	I - II - III	MIN.	0.25	V
I_{GD}		I - II - III	MIN.	3	mA
I_H(2)	I_T = 1000 mA	I - II - III	MAX.	120	mA
I_L	I_G = 1.2 I_{GT}	I - II - III	MAX.	300	mA
dV/dt(2)	V_D = 66.7% V_{DRM}, gate open , T_j = 125°C		MIN.	1000	V/µs
V_{INS}	Insulation voltage, AC 50 HZ ; R.M.S. ; 1s/60s			3000/2500	V

STATIC CHARACTERISTICS					
SYMBOL	TEST CONDITIONS			VALUE	UNIT
V_{TM}(2)	I_{TM} = 100 A, t_P = 380 µs	T_j = 25°C	MAX.	1.35	V
V_{t0}(2)	Threshold voltage	T_j = 125°C	MAX.	0.8	V
R_d(2)	Dynamic resistance	T_j = 125°C	MAX.	10	mΩ
I_{DRM} I_{RRM}	V_D = V_{DRM} V_R = V_{RRM}	T_j = 25°C	MAX.	0.5	mA
		T_j = 125°C		10	mA

Note 1: Minimum I_{GT} is guaranted at 5% of I_{GT} max.
Note 2: For both polarities of A2 referenced to A1.

THERMAL RESISTANCE			
SYMBOL	TEST CONDITIONS	VALUE	UNIT
$R_{th(j-c)}$	Junction to DBC (AC)	0.28	°C/W
$R_{th(j-s)}$	cont.per thyristor	1.2	K/W
	Sin.180° per thyristor	1.24	K/W
	ont.per W1C	0.6	K/W
	Sin.180° per W1C	0.62	K/W

PRODUCT SELECTOR					
PART NUMBER	VOLTAGE (xx)		SENSITIVITY	TYPE	PACKAGE
	1200V	1600V			
100KQxxK	V	V	80 mA	Snubberless	DBC module

ORDERING INFORMATION					
ORDERING TYPE	MARKING	PACKAGE	WEIGHT	BASE Q'TY	DELIVERY MODE
100KQxxK	100KQxxK	DBC module	13g	50	Box

Note: xx = voltage

ORDERING INFORMATION SCHEME

100 KQ 12 K

Current, $I_{T(RMS)}$
100 = 100A

SCR series
Antiparallel Thyristor

Voltage
12 = 1200V
16 = 1600V

Package type
K = DBC module (open-frame)

Fig.1 Maximum power dissipation versus on-state RMS current (full cycle)

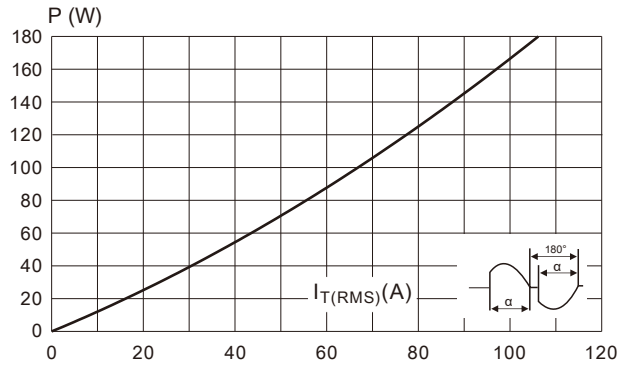


Fig.2 On-state rms current versus case temperature (full cycle)

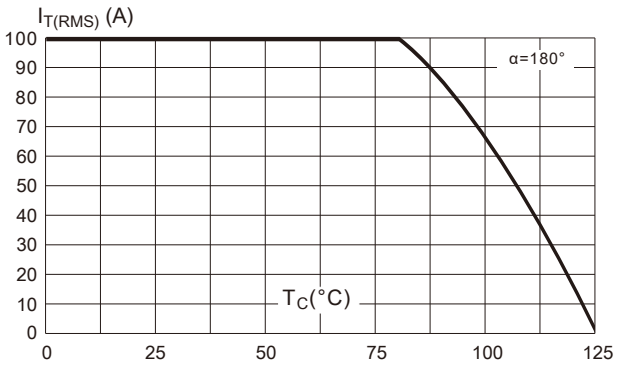


Fig.3 On-state characteristics (maximum values).

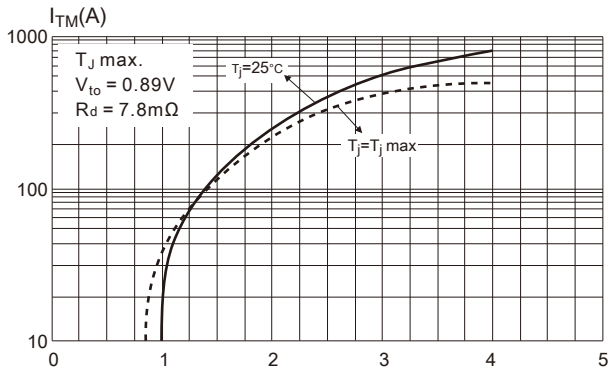


Fig.4 Surge peak on-state current versus number of cycles.

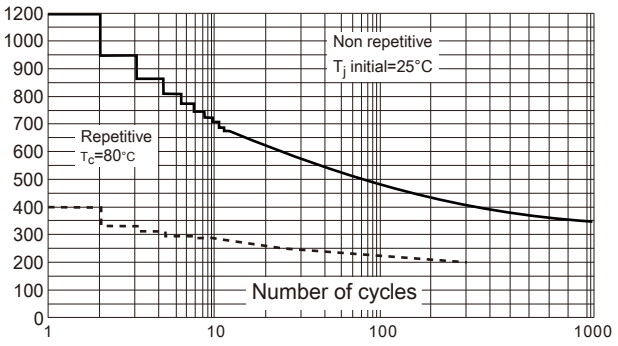


Fig.5 Non-repetitive surge peak on-state current for a sinusoidal pulse and corresponding value of I^2t.

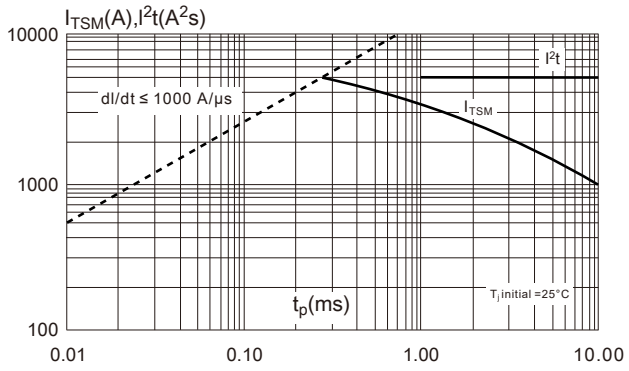
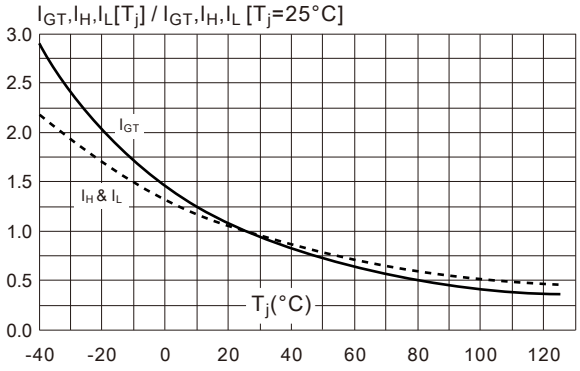
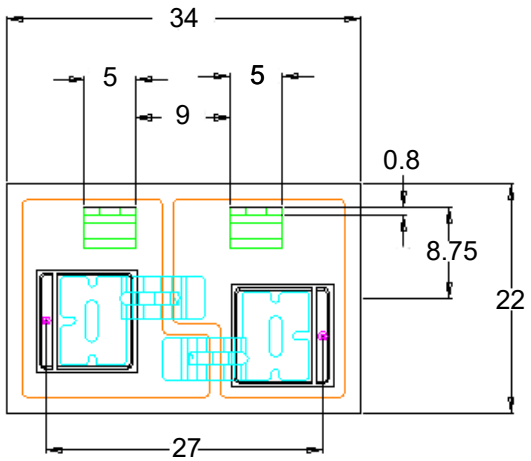
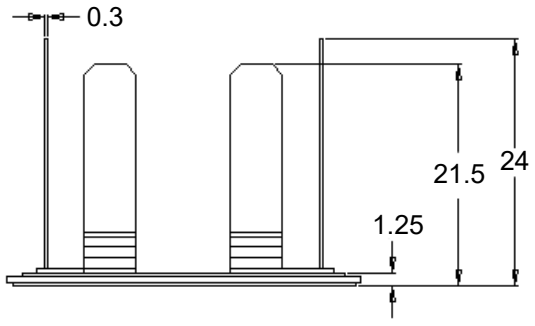


Fig.6 Relative variation of gate trigger, holding and latching current versus junction temperature (typical values)



Case Style





All dimensions in millimeters